AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A bi-directional shift controller comprising:

a first control line with a first voltage;

a second control line with a second voltage;

a plurality of transistors serially connected between said ~~a~~ first control line and a third voltage, wherein a source ~~the second~~ terminal of a ~~the~~ first transistor is electrically connected to said first control line and a ~~the~~ drain terminal of said first transistor is electrically connected to a ~~the~~ second transistor, and a ~~the~~ source terminal of a ~~the~~ third transistor is connected to said third voltage;

a fourth transistor connected between said ~~a~~ second control line and an input terminal of a shift register stage, the drain terminal of said first transistor further electrically connected to said input terminal of said shift register stage;

means to apply a first output voltage from previous shift register stage concurrently to gate terminals of each of said first and third transistors; and

means to apply a second output voltage from next shift register stage concurrently to gate terminals of each of said second and fourth transistors.

2. (Previously presented) The bi-directional shift controller as recited in claim 1, further comprising:

means to invert said first and second voltages.

3. (Previously presented) The bi-directional shift controller as recited in claim 1, wherein said first, second, third, and fourth transistors provide a combinatorial logic ~~is~~ operable as a NOR gate.

4. (Previously presented) The bi-directional shift controller as recited in claim 3, wherein said first and fourth transistors are n-type and said second and third transistors are p-type.

5. (Previously presented) The bi-directional shift controller as recited in claim 3, wherein said third voltage is V_{dd}.

6. (Previously presented) The bi-directional shift controller as recited in claim 5, wherein said first control line voltage is V_{dd} and second control line voltage is V_{ss}, wherein V_{dd} is higher than V_{ss}.

7. (Previously presented) The bi-directional shift controller as recited in claim 5, wherein said first control line voltage is V_{ss} and second control line voltage is V_{dd}, wherein V_{dd} is higher than V_{ss}.

8. (Previously presented) The bi-directional shift controller as recited in claim 1, wherein said first, second, third, and fourth transistors provide a combinatorial logic operable as a NAND gate.

9. (Previously presented) The bi-directional shift controller as recited in claim 8, wherein said first and fourth transistors are p-type and said second and third transistors are n-type.

10. (Previously presented) The bi-directional shift controller as recited in claim 8, wherein said third voltage is V_{ss}.

11. (Previously presented) The bi-directional shift controller as recited in claim 10, wherein said first control line voltage is V_{dd} and second control line voltage is V_{ss}.

12. (Previously presented) The bi-directional shift controller as recited in claim10, wherein said first control line voltage is V_{ss} and second control line voltage is V_{dd}.

13. (Previously presented) The bi-directional shift controller as recited in claim 1, wherein said transistors are selected from the group consisting of field effect transistors and floating gate transistors.

14. (Previously presented) The bi-directional shift controller as recited in claim 1, wherein said shift register stages are physically adjacent to said bi-directional controller.

15. (Previously presented) The bi-directional shift controller circuit as recited in claim 1, wherein said shift register stages are logically adjacent to said bi-directional controller.

16. (Currently Amended) A bi-directional shift register circuit comprising:

a first control line with a first voltage;

a second control line with a second voltage;

a plurality of shift register stages, each of the shift register stages having an input terminal and an output terminal, and

a bi-directional shift controller comprising:

a plurality of transistors serially connected between said ~~a~~ first control line and a third voltage, wherein a ~~the~~ source terminal of a ~~the~~ first transistor is electrically connected to said first control line, and a ~~the~~ drain terminal of said first transistor is electrically connected to a ~~the~~ second transistor, and a ~~the~~ source terminal of a ~~the~~ third transistor is connected to said third voltage;

a ~~the~~ fourth transistor connected between said ~~a~~ second control line and an input terminal of a shift register stage, the drain terminal of said first transistor further electrically connected to said input terminal of said shift register stage;

means to apply a first output voltage from previous shift register stage concurrently to gate terminals of each of said first and third transistors; and

means to apply a second output voltage from next shift register stage concurrently to gate terminals of each of said second and fourth transistors.

17. (Canceled)

18. (Previously presented) The bi-directional shift register circuit as recited in claim 16, further comprising:

means to invert voltages on said first and second inputs.

19. (Previously presented) The bi-directional shift register circuit as recited in claim 16 wherein said first, second, third, and fourth transistors provide a combinatorial circuit operable as an NOR gate.

20. (Previously presented) The bi-directional shift controller as recited in claim 19, wherein said first and fourth transistors are n-type and said second and third transistors are p-type.

21. (Previously presented) The bi-directional shift controller circuit as recited in claim 19, wherein said third voltage is V_{dd}.

22. (Previously presented) The bi-directional shift controller circuit as recited in claim 21, wherein said first control line voltage is V_{dd} and second control line voltage is V_{ss}, wherein V_{dd} is higher than V_{ss}.

23. (Previously presented) The bi-directional shift controller circuit as recited in claim 21, wherein said first control line voltage is V_{ss} and second control line voltage is V_{dd}, wherein V_{dd} is higher than V_{ss}.

24. (Previously presented) The bi-directional shift controller circuit as recited in claim 16, wherein said first, second, third, and fourth transistors provide a combinatorial logic operable as a NAND gate.

25. (Previously presented) The bi-directional shift controller circuit as recited in claim 24, wherein said first and fourth transistors are p-type and said second and third transistors are n-type.

26. (Previously presented) The bi-directional shift controller circuit as recited in claim 24, wherein said third voltage is V_{ss}.

27. (Previously presented) The bi-directional shift controller circuit as recited in claim 26, wherein said first control line voltage is V_{dd} and second control line voltage is V_{ss}.

28. (Previously presented) The bi-directional shift controller circuit as recited in claim 26, wherein said first control line voltage is V_{ss} and second control line voltage is V_{dd}.

29. (Previously presented) The bi-directional shift controller circuit as recited in claim 16, wherein said transistors are selected from the group consisting of field effect transistors and floating gate transistors.

30. (Previously presented) The bi-directional shift controller circuit as recited in claim 16, wherein said shift register stages are physically adjacent to said bi-directional controller.

31. (Previously presented) The bi-directional shift controller circuit as recited in claim 16, wherein said shift register stages are logically adjacent to said bi-directional controller.